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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,325	09/23/2005	Hiroshi Jiken	1110/95342	2064

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

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02/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,325	JIKEN ET AL.	
	Examiner	Art Unit	
	SAMUEL A. GEBREMARIAM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/04/08;09/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

2. Figures 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what the structural relationship is between an epitaxial layer, plural epitaxial layers, one of the plural epitaxial layer and other epitaxial layers as recited in claims 5-10.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 5-7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Toeda JP,06-163556A.

Regarding claim 5, as best the examiner is able to ascertain the claimed invention Toeda teaches (fig. 1) a semiconductor epitaxial wafer (fig. 1) having an epitaxial layer (2,3) stacked on a semiconductor substrate (1), wherein: plural epitaxial layers (2,3) are stacked on a front side (upper surface of 1) of the semiconductor substrate (1); and an impurity concentration of any one of the plural epitaxial layers (2) is high enough to afford a latch-up resistance (refer to the abstract) and a high-frequency conformity and is higher than impurity concentrations of the semiconductor substrate (1) and other epitaxial layers (3).

Regarding claim 6, as best the examiner is able to ascertain the claimed invention Toeda teaches a semiconductor epitaxial wafer (fig. 1) having an epitaxial layer (2,3) stacked on a semiconductor substrate (1), wherein: plural epitaxial layers (2,3) are stacked on a front side of the semiconductor substrate (1); an impurity concentration of any one of the plural epitaxial layers (2) is high enough for the formation of a gettering site and is higher than impurity concentrations of the semiconductor substrate (1) and other epitaxial layers (3); and an impurity concentration

of the semiconductor substrate (1) is at a level of suppressing impurity discharge from the semiconductor substrate (refer to the abstract).

Regarding claim 7, Toeda teaches the entire claimed structure of claim 5 above including an impurity concentration of the epitaxial layer (2) being in contact with the semiconductor substrate (1) among the plural epitaxial layers (2,3) is higher than the impurity concentrations of the semiconductor substrate (1) and the other epitaxial layers (3).

Regarding claim 10, Toeda teaches the entire claimed structure of claim 5 above including a high-concentration epitaxial layer (2) among the plural epitaxial layers contains boron (refer to paragraph 0007 of the attached computer translation).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toeda in view of Asano et al., US2003/0197190.

Regarding claim 8, as best the examiner is able to ascertain the claimed invention, Toeda teaches a semiconductor epitaxial wafer having an epitaxial layer (2,3) stacked on a semiconductor substrate (1), wherein: plural epitaxial layers (2,3) are stacked on a front side of the semiconductor substrate (1); an impurity concentration of

a high-concentration epitaxial layer among the plural epitaxial layers is 8x1018 (atoms/cm3 refer to paragraph 0008).

How Toeda does not explicitly teaches that an impurity concentration of the semiconductor substrate is 1.22x I 014 to 1.46x 1016 (atoms/cm3).

Asano teaches the use of a semiconductor substrate (10) having an impurity concentration of 1x1014 to 1x1018/cm3 in the structure of a semiconductor device with reduced parasitic capacitance.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the substrate taught by Asano in the structure of Toeda in order to form a device with reduced parasitic capacitance.

Regarding claim 9, as best the examiner is able to ascertain the claimed invention, the combined structure of Toeda and Asano teaches a semiconductor epitaxial wafer having an epitaxial layer (2,3) stacked on a semiconductor substrate (1), wherein: plural epitaxial layers (2,3) are stacked on a front side of the semiconductor substrate (1); a resistivity of a high-concentration epitaxial layer among the plural epitaxial layers is 0.002 to 0.1 (Ω-cm) (inherently the same); and a resistivity of the semiconductor substrate is 1 to 100 (Ω-cm, [0061], Asano).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
February 18, 2008

/Samuel A Gebremariam/
Examiner, Art Unit 2811